

**What is claimed is:**

1           1.    A flash memory device with selective gate  
2    within a substrate, comprising:

3           a substrate;

4           a floating gate disposed on the substrate;

5           a wordline extending along a first direction and  
6           overlying the floating gate and the adjacent  
7           substrate thereof;

8           a trench disposed in the substrate adjacent to one  
9           side of the wordline;

10          a selective gate vertically disposed in the trench  
11          and partially covering the floating gate;

12          a source region disposed in the substrate adjacent  
13          to the other side of the wordline; and

14          a drain region disposed in the substrate beneath the  
15          selective gate.

1           2.    The flash memory device as claimed in claim 1,  
2    wherein the floating gate further comprises a first  
3    dielectric layer and a first polysilicon layer,  
4    sequentially stacked on the substrate.

1           3.    The flash memory device as claimed in claim 2,  
2    further comprising an oxide layer with a width between  
3    130Å and 220Å disposed on both sides of the first  
4    polysilicon layer such that one thereof contacts the  
5    selective gate.

1           4.    The flash memory device as claimed in claim 1,  
2           further comprising a control gate formed by the portion  
3           of the wordline overlying the floating gate.

1           5.    The flash memory device as claimed in claim 1,  
2           wherein the wordline extends along a first direction is  
3           composed of a second dielectric layer, a second  
4           conductive layer and a cap layer.

1           6.    The flash memory device as claimed in claim 5,  
2           further comprising a spacer disposed on both sides of the  
3           cap layer.

1           7.    The flash memory device as claimed in claim 1,  
2           wherein the selective gate further comprises a third  
3           dielectric layer and a third conductive layer, and the  
4           third dielectric layer formed on one sidewall and  
5           portions of the bottom of the trench.

1           8.    The flash memory device as claimed in claim 1,  
2           wherein the trench extends along a first direction and  
3           has a depth between 800Å and 1200Å.

1           9.    The flash memory device as claimed in claim 7,  
2           wherein the third dielectric layer is between 120Å and  
3           200Å.

1           10.   The flash memory device as claimed in claim 7,  
2           wherein the third conductive layer is between 200Å and  
3           500Å.

1           11. A method of fabricating a flash memory device  
2 with selective gate within a substrate, comprising the  
3 steps of:

4           providing a substrate;

5           sequentially depositing a first dielectric layer and  
6           a first conductive layer on the substrate;

7           defining the first conductive layer, to form an  
8           active area extending along a first direction;

9           sequentially depositing a second dielectric layer, a  
10          second conductive layer and a cap layer on the  
11          substrate, and covering the active area;

12          defining the cap layer and the second conductive  
13          layer, to form a wordline pattern extending  
14          along a second direction and partially covering  
15          the active area;

16          forming a pair of spacers respectively disposed on  
17          both sides of the wordline pattern to form a  
18          wordline;

19          etching the second dielectric layer and the first  
20          conductive layer exposed by the wordline, to  
21          form a control gate within the portion of the  
22          wordline in the active area;

23          etching the substrate at one side of the wordline to  
24          form a trench therein;

25          forming a drain region in the substrate beneath the  
26          trench;

27          sequentially forming a third dielectric layer and a  
28          third conductive layer on one sidewall and  
29          portions of the bottom of the trench, and

30 partially covering the floating gate, to  
31 vertically form a selective gate in the trench;  
32 and  
33 forming a source region in the substrate at the  
34 other side of the wordline, and electrically  
35 contacting the floating gate.

1 12. The method as claimed in claim 11, wherein the  
2 method for forming the third dielectric layer is thermal  
3 oxidation.

1 13. The method as claimed in claim 12, wherein when  
2 forming the third dielectric layer, an oxide layer is  
3 formed on both sides of the second conductive layer  
4 within the floating gate.

1 14. The method as claimed in claim 13, wherein the  
2 oxide layer has a thickness between 130Å and 220Å.

1 15. The method as claimed in claim 11, wherein the  
2 trench has a depth between 800Å and 1200Å.

1 16. The method as claimed in claim 11, wherein the  
2 first direction is substantially perpendicular to the  
3 second direction.

1 17. The method as claimed in claim 11, wherein the  
2 third dielectric layer is formed on the sidewall and  
3 portions of the bottom of the trench.